LESSON PLAN

Subject Code & Name: 13EC3013 & DIGITAL IC APPLICATIONS **Branch: ECE**
Class / Semester: III B.Tech I Semester **Academic Year: 2017-18**

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks
		Unit-1 Logic Families			
1.	**13.06.2017**	Introduction to logic families	**1**	**BB & Chalk**	
2.	**14.06.2017**	CMOS logic	**1**	**BB & Chalk**	
3.	**15.06.2017**	CMOS steady state electrical behavior	**1**	**BB & Chalk**	
4.	**17.06.2017**	CMOS dynamic electrical behavior	**1**	**BB & Chalk**	
5.	**20.06.2017**	CMOS logic families	**1**	**BB & Chalk**	
6.	**21.06.2017**	bipolar logic	**1**	**BB & Chalk**	
7.	**22.06.2017**	diode Logic	**1**	**BB & Chalk**	
8.	**24.06.2017**	transistor logic	**1**	**BB & Chalk**	
9.	**27.06.2017**	TTL families	**1**	**BB & Chalk**	
10.	**28.06.2017**	CMOS/TTL interfacing,	**1**	**BB & Chalk**	
11.	**29.06.2017**	low voltage CMOS logic and interfacing	**1**	**BB & Chalk**	
12.	**01.07.2017**	emitter coupled logic	**1**	**BB & Chalk**	
13.	**12.07.2017**	comparison of logic families	**1**	**BB & Chalk**	
		Unit-2 Combinational Logic Design – I			
14.	**13.07.2017**	Design and analysis procedures of decoders	**2**	**BB & Chalk / LCD**	
15.	**15.07.2017**	Design and analysis procedures of encoders,	**2**	**BB & Chalk / LCD**	
16.	**18.07.2017**	Three state devices,	**2**	**BB & Chalk**	
17.	**19.07.2017**	multiplexers and de-multiplexers,	**2**	**BB & Chalk /LCD**	
18.	**20.07.2017**	EX-OR gates and parity circuits and comparators.	**2**	**BB & Chalk**	
19.	**22.07.2017**	Design considerations of the above combinational logic with relevant digital ICs.	**2**	**BB & Chalk**	
20.	**25.07.2017**	VHDL modeling of decoders,	**2**	**BB & Chalk**	
21.	**26.07.2017**	VHDL modeling of encoders,	**2**	**BB & Chalk**	
22.	**27.07.2017**	VHDL modeling of multiplexers	**2**	**BB & Chalk**	
23.	**29.07.2017**	VHDL modeling of comparators.	**2**	**BB & Chalk**	
		UNIT-III Combinational Logic Design – II			
24.	**01.08.2017**	Design and analysis procedures of adders,	**3**	**BB & Chalk /LCD**	
25.	**02.08.2017**	Subtractors	**3**	**BB & Chalk /LCD**	
26.	**03.08.2017**	ALUs	**3**	**BB & Chalk /LCD**	
27.	**05.08.2017**	barrel shifter	**3**	**BB & Chalk /LCD**	
28.	**08.08.2017**	simple floating-point encoder,	**3**	**BB & Chalk /LCD**	
29.	**09.08.2017**	dual parity encoder,	**3**	**BB & Chalk**	
30.	**10.08.2017**	cascading comparators	**3**	**BB & Chalk**	
31.	**12.08.2017**	Combinational multipliers. Design considerations of the	**3**	**BB & Chalk**	

		above combinational logic with relevant digital ICs.			
32.	**16.08.2017**	VHDL modeling of adders, subtractors,	**3**	**BB & Chalk**	
33.	**17.08.2017**	barrel shifter	**3**	**BB & Chalk**	
34.	**19.08.2017**	combinational multipliers	**3**	**BB & Chalk**	
		Unit-4 **Sequential Logic Design**			
35.	**22.08.2017**	Latches	**4**	**BB & Chalk**	
36.	**23.08.2017**	flip-flops	**4**	**BB & Chalk**	
37.	**24.08.2017**	Counters	**4**	**BB & Chalk /LCD**	
38.	**26.08.2017**	shift registers	**4**	**BB & Chalk /LCD**	
39.	**29.08.2017**	synchronous design methodology	**4**	**BB & Chalk**	
40.	**30.08.2017**	Impediments to synchronous design.	**4**	**BB & Chalk**	
41.	**31.08.2017**	VHDL modeling of ripple counters,	**4**	**BB & Chalk**	
42.	**05.09.2017**	synchronous counters	**4**	**BB & Chalk**	
43.	**06.09.2017**	shift registers	**4**	**BB & Chalk**	
		Unit-5 **PLDs**			
44.	**07.09.2017**	Introduction to PROM	**5**	**BB & Chalk**	
45.	**09.09.2017**	RAM	**5**	**BB & Chalk /LCD**	
46.	**13.09.2017**	PLA	**5**	**BB & Chalk /LCD**	
47.	**16.09.2017**	PAL	**5**	**BB & Chalk /LCD**	
48.	**21.09.2017**	CPLD	**5**	**BB & Chalk /LCD**	
49.	**23.09.2017**	FPGA	**5**	**BB & Chalk /LCD**	
50.	**03.09.2017**	Design considerations of PLDs with relevant digital ICs.	**5**	**BB & Chalk**	
51.	**04.10.2017**	VHDL modeling of memories	**5**	**BB & Chalk**	
52.	**05.10.2017**	VHDL modeling of PLDs	**5**	**BB & Chalk**	
53.	**07.10.2017**	Revision	**5**	**BB & Chalk**	

Faculty Name: III ECE-A : Smt. E.Jaya III ECE-B : Dr. B. Chinna Rao III ECE-C : Sri M.L. Naidu

CR: CLASS ROOM BB: BLACK BOARD OHP: OVERHEAD PROJECTOR LCD

Text books:

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 2005, 3/e.
2. Digital IC Applications – Atul P.Godse and Deepali A.Godse, Technical Publications, Pune, 2005.
3. VHDL Primer – J. Bhasker, PHI,3rd Edition.

Reference books:

1. Digital System Design Using VHDL – Charles H. Roth Jr., PWS Publications,1998.
2. Digital Logic and Computer Design by Morris Mano, Prentice Hall.

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