# LESSON PLAN

| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action Upon Review |
|---|---|---|---|---|---|---|
| 1 | 12/06/17 | Introduction to logic families | I | Black board | | |
| 2 | 14/06/17 | CMOS logic NAND | | " | | |
| 3 | 16/06/17 | CMOS NOR, NOT | | " | | |
| 4 | 17/06/17 | CMOS AND, OR. | | " | | |
| 5 | 19/06/17 | CMOS Different gates | | " | | |
| 6 | 21/06/17 | CMOS steady state electric. behaviour | | " | | |
| 7 | 23/06/17 | " | | " | | |
| 8 | 24/06/17 | CMOS dynamic electrical behaviour | | " | | |
| 9 | 28/06/17 | CMOS logic families | | " | | |
| 10 | 30/06/17 | Bipolar logic, diode logic | | " | | |
| 11 | 01/07/17 | transistor logic | | " | | |
| 12 | 03/07/17 | TTL families. | | " | | |
| 13 | 05/07/17 | " | | " | | |
| 14 | 07/07/17 | CMOS / TTL interfacing | | " | | |
| 15 | 08/07/17 | Low voltage CMOS logic and interfacing | | " | | |
| 16 | 10/07/17 | Emitter coupled logic | | " | | |
| 17 | 12/07/17 | " | | " | | |
| 18 | 14/07/17 | Comparision of logic families | | " | | |
| 19 | 15/07/17 | Design and analysis procedures of Encoders | II | " | | |

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|---|---|---|---|---|---|---|
| 20 | 17/07/17 | " | II | Black Board | | |
| 21 | 19/07/17 | encoders | | " | | |
| 22 | 21/07/17 | } 1st unit Exam | | " | | |
| 23 | 24/07/17 | | | " | | |
| 24 | 24/07/17 | Encoders. | | " | | |
| 25 | 26/07/17 | Three state devices | | " | | |
| 26 | 28/07/17 | multiplexers. | | " | | |
| 27 | 29/07/17 | " | | " | | |
| 28 | 31/07/17 | Demultiplexers | | " | | |
| 29 | 02/08/17 | Ex-OR gates | | " | | |
| 30 | 04/08/17 | parity circuits | | " | | |
| 31 | 05/08/17 | Comparators | | " | | |
| 32 | 07/08/17 | IC's | | " | | |
| 33 | 09/08/17 | VHDL modeling of Decoders | | " | | |
| 34 | 11/08/17 | VHDL modeling of encoders | | " | | |
| 35 | 12/08/17 | VHDL modeling of mux and comparators | | " | | |
| 36 | 14/08/17 | Design and analysis procedures of adders | III | " | | |
| 37 | 16/08/17 | Subtractors | | " | | |
| 38 | 18/08/17 | ALU's | | " | | |
| 39 | 19/08/17 | Barrel Shifters | | " | | |

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|---|---|---|---|---|---|---|
| 40 | 21/08/17 | Simple floating point encoder | III | Black board | | |
| 41 | 23/08/17 | Quad parity encoder | | " | | |
| 42 | 28/08/17 | Cascading comparators & combinational ckts | | " | | |
| 43 | 29/08/17 | All with Relevant diagrams | | " | | |
| 44 | 30/08/17 | I Mid Exam | | " | | |
| 45 | 01/09/17 | | | " | | |
| 46 | 04/09/17 | VHDL modeling of Adders | | " | | |
| 47 | 06/09/17 | VHDL modeling of subtractors | | " | | |
| 48 | 08/09/17 | VHDL modeling of barrel shifters & error | | " | | |
| 49 | 09/09/17 | Latches & flipflops | IV | " | | |
| 50 | 11/09/17 | " | | " | | |
| 51 | 13/09/17 | Counters | | " | | |
| 52 | 15/09/17 | Shift Registers | | " | | |
| 53 | 16/09/17 | Synchronous design methodology | | " | | |
| 54 | 18/09/17 | Implementation of Synchronous FSM | | " | | |
| 55 | 20/09/17 | VHDL modeling of Sequential circuits | | " | | |
| 56 | 22/09/17 | Synchronous counters and | | " | | |
| 57 | 23/09/17 | Shift registers | | " | | |
| 58 | 25/09/17 | Introduction to PROMs | V | " | | |
| 59 | 27/09/17 | RAM | | " | | |

# LESSON PLAN

| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action Upon Review |
|---|---|---|---|---|---|---|
| 60 | [illegible] | RA | V | Black Board | | |
| 61 | [illegible] | PAL | " | " | | |
| 62 | [illegible] | CPLD | | " | | |
| 63 | [illegible] | FPGA | | " | | |
| 64 | [illegible] | Design considerations of PLD with ICs | | " | | |
| 65 | [illegible] | VHDL modelling of [illegible] | | " | | |
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