LESSON PLAN

Subject Name: COMPUTER ORGANIZATION AND ARCHITECTURE
Subject Code : 13CS3008 **Branch: ECE-B**
Class / Semester: III B.Tech I Semester **Academic Year: 2017-18**

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks
		Unit-1			
1.	13.0617	**Introduction:** Basics of computer and its applications.	**1**	**CR**	
2.	14.06.17	Fundamental concepts of design methodologies;		**CR**	
3.	15.06.17	Basic organization of computer.		**CR**	
4.	17.06.17	Computer types, functional unit and its importance.		**CR**	
5.	20.06.17	Basic operational concepts,		**CR**	
6.	21.06.17	Types of Bus structures, software, performance measurements.		**CR**	
7.	22.06.17	Explanation and examples of Multiprocessors and multi computers.		**CR**	
8.	24.06.17	Data representation: fixed point representation with some examples floating point representation. Problems and solutions		**CR**	
9.	27.06.17	Data representation: floating point representation with some examples		**CR**	
10.	28.06.17	Problems and solutions		**CR**	
		Unit-2			
11.	29.06.17	**Computer Arithmetic:** Explanation of Addition and subtraction algorithms	**2**	**CR**	
12.	01.07.17	Problems and Solutions		**CR**	
13.	11.07.17	Multiplication algorithms and its explanation		**CR**	
14.	12.07.17	Division algorithms and its explanation		**CR**	
15.	13.07.17	Problems and Solutions		**CR**	
16.	15.07.17	Examples on Addition, Subtraction, Multiplication and Division		**CR**	
17.	18.07.17	Fixed and floating – point arithmetic operations with examples		**CR**	
18.	19.07.17	Decimal arithmetic unit and decimal arithmetic operations		**CR**	
19.	25.07.17	Problems and Solutions		**CR**	
20.	26.07.17	Problems and Solutions		**CR**	
		Unit-3			
21.	27.07.17	**Register Organization, Machine Instruction set:** Register transfer language	**3**	**CR**	
22	29.07.17	Register transfer bus and memory transfers		**CR**	
23.	01.08.17	Arithmetic micro-operations		**CR**	
24.	02.08.17	Logic micro operations		**CR**	
25.	03.08.17	Shift micro operations		**CR**	
26.	05.08.17	Arithmetic logic shift unit-Explanation		**CR**	
27.	08.08.17	Instruction codes-Examples		**CR**	
28.	09.08.17	General register Organization, Control word		**CR**	
29.	10.08.17	Computer instructions: Instruction Format and Instruction cycle		**CR**	
30.	16.08.17	Addressing Modes with Examples		**CR**	
31.	17.08.17	Processor organization, RISC and CISC characteristics		**CR**	

		Unit-4			
32	**18.08.17**	**Memory System:** Memory hierarchy, main memory-Explanation	**4**	**CR**	
33	**19.08.17**	Auxiliary memory, Associative memory-Explanation		**CR**	
34	**22.08.17**	Hardware organization, Match logic, Read and Write operations		**CR**	
35	**23.08.17**	Cache memory, Associative and direct mapping concepts		**CR**	
36	**24.08.17**	Cache initialization and writing into cache		**CR**	
37.	**26.08.17**	Virtual memory concept and its importance		**CR**	
38.	**29.08.17**	Memory management hardware, memory protection		**CR**	
39.	**05.09.17**	**Input – Output Organization:** Peripheral devices-Explanation		**CR**	
40.	**06.09.17**	Input – Output Organization: input-output interface-examples		**CR**	
41.	**07.09.17**	Asynchronous data transfer-modes of transfer		**CR**	
42.	**12.09.17**	Example of programmed I/O and Interrupt-Initiated I/O		**CR**	
43.	**13.09.17**	Interrupts-Types and Priority Interrupt		**CR**	
44.	**14.09.17**	Direct memory access, DMA controller, DMA transfer		**CR**	
45.	**16.09.17**	Input – output processor (IOP) and serial communication		**CR**	
		Unit-5			
46.	**19.09.17**	**Pipeline:** Parallel processing-concepts and explanation	**5**	**CR**	
47.	**20.09.17**	Pipelining concepts. Arithmetic pipeline, instruction pipeline		**CR**	
48.	**21.09.17**	RISC pipeline with examples.		**CR**	
49.	**23.09.17**	**Multi processors:** Characteristics of multiprocessors and its applications		**CR**	
50.	**26.09.17**	Interconnection structures in detail		**CR**	
51.	**04.10.17**	Interprocessor arbitration: system bus, Serial arbitration procedure		**CR**	
52.	**05.10.17**	Interprocessor communication and synchronization		**CR**	
53.	**07.10.17**	Mutual exclusion with a semaphore		**CR**	
54.	**10.10.17**	Concept of cache coherence in detail.		**CR**	
55.	**11.10.17**	Conditions for incoherence, solutions to the cache coherence problem -Previous papers review		**CR**	

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